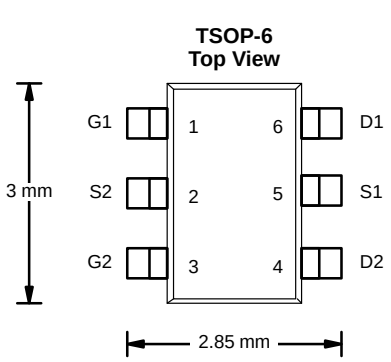
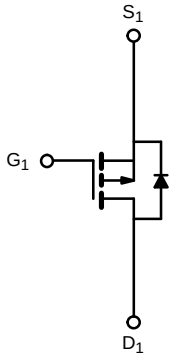
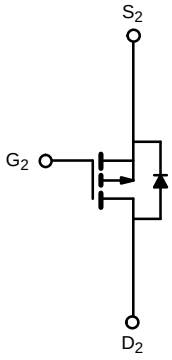
SI3905DV

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
–8	0.125 @ V_{GS} = –4.5 V	±2.5
	0.175 @ V_{GS} = –2.5 V	±2.0
	0.265 @ V_{GS} = –1.8 V	±1.7





P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	–8	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Drain Current (T_J = 150°C)[a, b]	T_A = 25°C	I_D	±2.5	A
	T_A = 70°C		±2.0	
Pulsed Drain Current		I_{DM}	±7	
Continuous Diode Current (Diode Conduction)[a, b]		I_S	–1.05	
Maximum Power Dissipation[a, b]	T_A = 25°C	P_D	1.15	W
	T_A = 70°C		0.73	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	93	110	°C/W
	Steady State		130	150	
Maximum Junction-to-Lead	Steady State	R_{thJL}	75	90	

Notes
a. Surface Mounted on FR4 Board.
b. t ≤ 5 sec

SI3905DV

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 μA	–0.45			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –6.4 V, V_{GS} = 0 V			–1	μA
		V_{DS} = –6.4 V, V_{GS} = 0 V, T_J = 55°C			–5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = ≤–5 V, V_{GS} = –4.5 V	–5			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = –2.5 A		0.103	0.125	Ω
		V_{GS} = –2.5 V, I_D = –2.0 A		0.146	0.175	
		V_{GS} = –1.8 V, I_D = –1 A		0.205	0.265	
Forward Transconductance[a]	g_{fs}	V_{DS} = –4.5 V, I_D = –2.5 A		5.3		S
Diode Forward Voltage[a]	V_{SD}	I_S = –1.05 A, V_{GS} = 0 V		–0.79	–1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = –5 V, V_{GS} = –4.5 V, I_D = –2.5 A		4.2	6	nC
Gate-Source Charge	Q_{gs}			0.45		
Gate-Drain Charge	Q_{gd}			0.90		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –5 V, R_L = 5 Ω I_D ≅ –1 A, V_{GEN} = –4.5 V, R_G = 6 Ω		10	15	ns
Rise Time	t_r			47	70	
Turn-Off Delay Time	$t_{d(off)}$			28	45	
Fall Time	t_f			34	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –1.05 A, di/dt = 100 A/μs		20	40	ns

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.